Abstract

The present invention provides a method for designing LSI including a logic circuit equipped with a scan circuit without generating a hard-macro library for the scan flip flops constituting the scan circuit. According to the method, first netlist NL1 is converted into second netlist NL2 by adding scan circuit including scan flip-flops. Order data for connecting scan chain of the scan circuit is extracted from the second netlist NL2. Such second netlist NL2 is converted into third netlist NL3 including only hard-macros, and the third netlist NL3 is laid-out by re-ordering the scan chain so that the newly generated order data for is stored temporally. Fourth netlist NL4 including scan circuit formed by scan flip-flops of soft-macros is generated on the basis of the stored order data, then the fourth netlist NL4 is converted into fifth netlist NL5 by substituting the scan flip-flops of soft-macros for standard cells of hard-macros. Finally the generated fifth netlist is laid-out without re-ordering the scan chain.